

1 added  
7.1  
device including data memory for storing digital test data output from the analog-to-digital converter circuit or digital test data produced by converting analog test data output from the digital-to-analog converter circuit into a digital signal, and an analysis section for analyzing the digital test data stored in the data memory; wherein the data memory is divided into two memory sections such that, when digital test data is stored in one memory section, digital test data previously stored in the other memory section is loaded for analysis purpose.

2. (Amended) The apparatus for testing a semiconductor integrated circuit according to claim 1, wherein the data memory has first and second memory devices, and the first and second memory devices respectively include the first and second memory sections.

Please add new claims 7-12 as follows:

7. (New) A method of testing a semiconductor integrated circuit, the semiconductor integrated circuit including at least one of an analog-to-digital converter circuit for converting an analog signal to a digital signal and a digital-to-analog converter circuit for converting a digital signal to an analog signal, the method using a test circuit board configured to exchange one or more signals with the semiconductor integrated circuit and a test ancillary device coupled to the test circuit board and including a memory having a first and second sections, the method comprising:

storing first digital test data derived from the semiconductor integrated circuit in the first memory section while providing second digital test data derived from the semiconductor integrated circuit and data previously stored in the second memory section to an analysis device configured to analyze digital test data stored in the data memory;

wherein the first and second digital test data are one of an output from the analog-to-digital converter circuit or digital test data produced by converting analog test data output from the digital-to-analog converter circuit into a digital signal.

7 8. (New) The method of claim <sup>6</sup>7, wherein the semiconductor integrated circuit includes both an analog-to-digital converter circuit and digital-to-analog converter circuit, and the test ancillary device is configured to alternatively store digital test data derived from the analog-to-digital converter circuit in a first mode of operation and digital test data derived from the digital-to-analog converter circuit in a second mode of operation.

8 9. (New) The method of claim <sup>6</sup>7, further comprising providing a source analog signal to the semiconductor integrated circuit, wherein the digital test data stored in the test ancillary device memory is derived from the analog-to-digital converter circuit converting the source analog signal to digital form.

9 10. (New) The method of claim <sup>6</sup>7, further comprising providing a source digital signal to the semiconductor integrated circuit, wherein the digital test data stored in the test ancillary device memory is derived from the digital-to-analog converter circuit converting the source digital signal to analog form.

11. (New) The method of claim 7, further comprising performing a changeover operation on the test ancillary device memory such that additional digital test data can be stored in the second memory section while the first digital test data is provided to the analysis device.